

## Claims

What is claimed is:

- 1           1.     Apparatus for enhanced timing loop for a partial-response  
2 maximum-likelihood (PRML) data channel in a direct access storage device  
3 (DASD) comprising:  
4           an acquisition timing circuit for generating an acquisition timing signal;  
5           said acquisition timing circuit including a plurality of compare functions  
6 for receiving and comparing consecutive input signal samples on an  
7 interleave with a threshold value;  
8           said acquisition timing circuit including a majority rule voting function  
9 coupled to said plurality of compare functions for selecting a timing  
10 interleave.
- 1           2.     Apparatus for enhanced timing loop for a partial-response  
2 maximum-likelihood (PRML) data channel as recited in claim 1 wherein said  
3 acquisition timing circuit includes three compare functions for receiving and  
4 comparing three consecutive input signal samples on said interleave with  
5 said threshold value.
- 1           3.     Apparatus for enhanced timing loop for a partial-response  
2 maximum-likelihood (PRML) data channel as recited in claim 2 wherein said  
3 majority rule voting function includes a two of three voting function coupled  
4 to said plurality of compare functions for selecting said timing interleave.
- 1           4.     Apparatus for enhanced timing loop for a partial-response  
2 maximum-likelihood (PRML) data channel as recited in claim 1 further  
3 includes tracking timing circuitry for generating a timing error signal during a  
4 read operation.
- 1           5.     Apparatus for enhanced timing loop for a partial-response  
2 maximum-likelihood (PRML) data channel as recited in claim 4 wherein said  
3 tracking timing circuitry includes a channel data detector, said channel data  
4 detector receiving disk signal input samples and including a multiple-state  
5 path memory.

1           6.     Apparatus for enhanced timing loop for a partial-response  
2 maximum-likelihood (PRML) data channel as recited in claim 5 wherein said  
3 tracking timing circuitry further includes a low latency detector receiving disk  
4 signal input samples.

1           7.     Apparatus for enhanced timing loop for a partial-response  
2 maximum-likelihood (PRML) data channel as recited in claim 6 wherein said  
3 tracking timing circuitry further includes a selector function coupled to an  
4 output of said low latency detector and coupled to said multiple-state path  
5 memory for selecting a state and utilizing said low latency detector output to  
6 select a state of said path memory and said selector function providing a low  
7 latency output corresponding to said selected state.

1           8.     Apparatus for enhanced timing loop for a partial-response  
2 maximum-likelihood (PRML) data channel as recited in claim 7 wherein said  
3 low latency output is used for generating said timing error signal during a  
4 read operation.

1           9.     Apparatus for enhanced timing loop for a partial-response  
2 maximum-likelihood (PRML) data channel as recited in claim 7 wherein said  
3 low latency output is applied to a convert-to-estimated sample function for  
4 generating an estimated sample and said estimated sample subtracted from  
5 said disk signal input samples for generating said timing error signal during a  
6 read operation.

1           10. A method for enhanced timing loop for a partial-response  
2 maximum-likelihood (PRML) data channel in a direct access storage device  
3 (DASD) comprising the steps of:  
4           receiving and comparing multiple consecutive input signal samples on  
5 an interleave with a threshold value;  
6           applying a majority rule voting function and selecting a timing  
7 interleave for an acquisition timing signal;  
8           during a read operation, applying disk signal input samples to a  
9 channel data detector and to a low latency data detector; said channel data  
10 detector including a multiple-state path memory;  
11           utilizing an output of said low latency detector for selecting a state of  
12 said multiple-state path memory and providing a low latency output  
13 corresponding to said selected state; and  
14           utilizing said low latency output for generating said timing error signal  
15 during said read operation.

1           11. A method for enhanced timing loop for a partial-response  
2 maximum-likelihood (PRML) data channel as recited in claim 10 wherein the  
3 step of receiving and comparing multiple consecutive input signal samples  
4 on an interleave with a threshold value includes the step of receiving and  
5 comparing three consecutive input signal samples on said interleave with  
6 said threshold value.

1           12. A method for enhanced timing loop for a partial-response  
2 maximum-likelihood (PRML) data channel as recited in claim 11 includes the  
3 step of identifying a zero or a one value for said three consecutive input  
4 signal samples.

1           13. A method for enhanced timing loop for a partial-response  
2 maximum-likelihood (PRML) data channel as recited in claim 10 wherein the  
3 step of applying a majority rule voting function and selecting a timing  
4 interleave for an acquisition timing signal includes the step of applying a two  
5 out of three voting function and selecting said timing interleave for said  
6 acquisition timing signal.

1           14.    A method for enhanced timing loop for a partial-response  
2   maximum-likelihood (PRML) data channel as recited in claim 10 wherein the  
3   step of utilizing an output of said low latency detector for selecting a state of  
4   said multiple-state path memory and providing a low latency output  
5   corresponding to said selected state includes the step of selecting a low  
6   latency state of said multiple-state path memory and providing said low  
7   latency output.

1           15.    A method for enhanced timing loop for a partial-response  
2   maximum-likelihood (PRML) data channel as recited in claim 10 wherein the  
3   step of utilizing said low latency output for generating said timing error signal  
4   during said read operation includes the steps of converting said low latency  
5   output to an estimated sample output and subtracting said estimated sample  
6   output from said disk signal input samples for generating said timing error  
7   signal during said read operation.

1           16.    Apparatus for enhanced timing loop for a partial-response  
2   maximum-likelihood (PRML) data channel in a direct access storage device  
3   (DASD) comprising:  
4           tracking timing circuitry for generating a timing error signal during a  
5   read operation; said tracking timing circuit including a channel data detector,  
6   said channel data detector receiving disk signal input samples and including  
7   a multiple-state path memory;  
8           said tracking timing circuit including a low latency detector receiving  
9   disk signal input samples;  
10          said tracking timing circuit including a selector function coupled to an  
11   output of said low latency detector and coupled to said multiple-state path  
12   memory for selecting a state and said selector function utilizing said low  
13   latency detector output for selecting said state of said path memory and for  
14   providing a low latency output corresponding to said selected state; and  
15          said low latency output being used for generating said timing error  
16   signal during a read operation.

1           17. Apparatus for enhanced timing loop for a partial-response  
2 maximum-likelihood (PRML) data channel as recited in claim 16 includes a  
3 convert-to-estimated sample function receiving said low latency output and  
4 generating an estimated sample and said estimated sample subtracted from  
5 said disk signal input samples for generating said timing error signal during a  
6 read operation.

1           18. Apparatus for enhanced timing loop for a partial-response  
2 maximum-likelihood (PRML) data channel as recited in claim 16 wherein  
3 said low latency detector includes a 4-state Viterbi detector.

1           19. Apparatus for enhanced timing loop for a partial-response  
2 maximum-likelihood (PRML) data channel as recited in claim 16 wherein  
3 said low latency output is less than a latency of an output of said channel  
4 data detector.

1           20. Apparatus for enhanced timing loop for a partial-response  
2 maximum-likelihood (PRML) data channel as recited in claim 16 includes an  
3 acquisition timing circuit for generating an acquisition timing signal; said  
4 acquisition timing circuit including a plurality of compare functions for  
5 receiving and comparing consecutive input signal samples on an interleave  
6 with a threshold value, and a majority rule voting function coupled to said  
7 plurality of compare functions for selecting a timing interleave.